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PROCESS OPTIONS OF FORMING SILICIDED METAL GATES FOR ADVANCED CMOS DEVICES

Abstract

Silicide is introduced into the gate region of a CMOS device through different process options for both conventional and replacement gate types processes. Placement of silicide in the gate itself, introduction of the silicide directly in contact with the gate dielectric, introduction of the silicide as a fill on top of a metal gate all ready in place, and introduction the silicide as a capping layer on polysilicon or on the existing metal gate, are presented. Silicide is used as an option to connect between PFET and NFET devices of a CMOS structure. The processes protect the metal gate while allowing for the source and drain silicide to be of a different silicide than the gate silicide. A semiconducting substrate is provided having a gate with a source and a drain region. A gate dielectric layer is deposited on the substrate, along with a metal gate layer. The metal gate layer is then capped with a silicide formed on top of the gate, and conventional formation of the device then proceeds. A second silicide may be employed within the

gate. A replacement gate is made from two different metals (dual metal gate replacement) prior to capping with a silicide.